PVP 14

Code: CS4T5

II B. Tech II Semester Regular/Supplementary Examinations
October - 2020

COMPUTER ORGANIZATION
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks
11 x 2 = 22 M

1.

a) Write the complement of Boolean expression (A + A' (B'C+BC')).
b) Describe SR Flip-Flop with its characteristic table.
c) Describe the fields of basic instruction format.
d) Differentiate Direct and Indirect addressing modes.
e) Explain asynchronous data transfer in strobe control method.
f) Define interrupt. List the ways to handle the interrupts.
g) Draw the block diagram of RAM 128 X 8 RAM chip.
h) Define mapping. List the types of mapping techniques in cache memory organization.
i) Describe associative memory.
j) List types of physical forms available for establishing interconnection network.
k) Define mutual exclusion and explain the use of semaphore in it.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Simplify the following Boolean function using four-variable K-map.
F(A, B, C, D) = $\sum$ (0,1,2,4,5,7,11,15) 8 M

b) Explain the design process of Full-adder with the help of truth table and maps. 8 M

3. a) Explain the evaluation process of the following expression using stack organization.
(A * B) + (C * D) 4 M

b) Explain any four addressing modes with numerical example. 8 M

c) Write Three-Address instructions to evaluate the following expression. X = (A + B) * (C + D) 4 M

4. a) Explain the purpose I/O interfaces between internal storage and external I/O devices. 4 M

b) Describe the handshaking method of asynchronous data transfer. 6 M

c) Explain Daisy-Chaining method to handle the interrupts. 6 M

5. a) Explain Auxiliary memories with its operational concepts. 8 M

b) Explain Virtual memory mapping process with neat sketch. 8 M

6. Write short note on the following

a) Crossbar switch. 5 M
b) Parallel bus arbitration. 6 M
c) Interprocessor synchronization. 5 M